Features

- **Low-voltage and Standard-voltage Operation, VCC = 2.7V–5.5V**
- **Internally Organized 65,536 x 8**
- **Two-wire Serial Interface**
- **Schmitt Triggers, Filtered Inputs for Noise Suppression**
- **Bidirectional Data Transfer Protocol**
- **1 MHz (5V) and 400 kHz (2.7V) Compatibility**
- **128-byte Page Write Mode (Partial Page Writes Allowed)**
- **Self-timed Write Cycle (5 ms Max)**
- **High Reliability**
  - **Endurance: 100,000 Write Cycles**
  - **Data Retention: 40 Years**
  - **ESD Protection: >4000V**

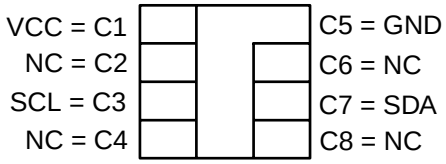
Description

The AT24C512SC provides 524,288 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 65,536 words of 8 bits each. This device is optimized for use in smart card applications where low-power and low-voltage operation may be essential. This device is available in a standard ISO 7816 smart card module (see *Ordering Information*, page 11). All devices are functionally equivalent to Atmel serial EEPROM products offered in standard IC packages (PDIP, SOIC, TSSOP, dBGA), with the exception of the slave address and write protect functions, which are not required for smart card applications.

Table 1. Pin Configurations

Pad Name	Description	ISO Module Contact
VCC	Power Supply Voltage	C1
GND	Ground	C5
SCL	Serial Clock Input	C3
SDA	Serial Data Input/Output	C7
NC	No Connect	C2, C4, C6, C8

Figure 1. Card Module Contact



Two-wire Serial EEPROM Smart Card Module 512K (65,536 x 8)

AT24C512SC

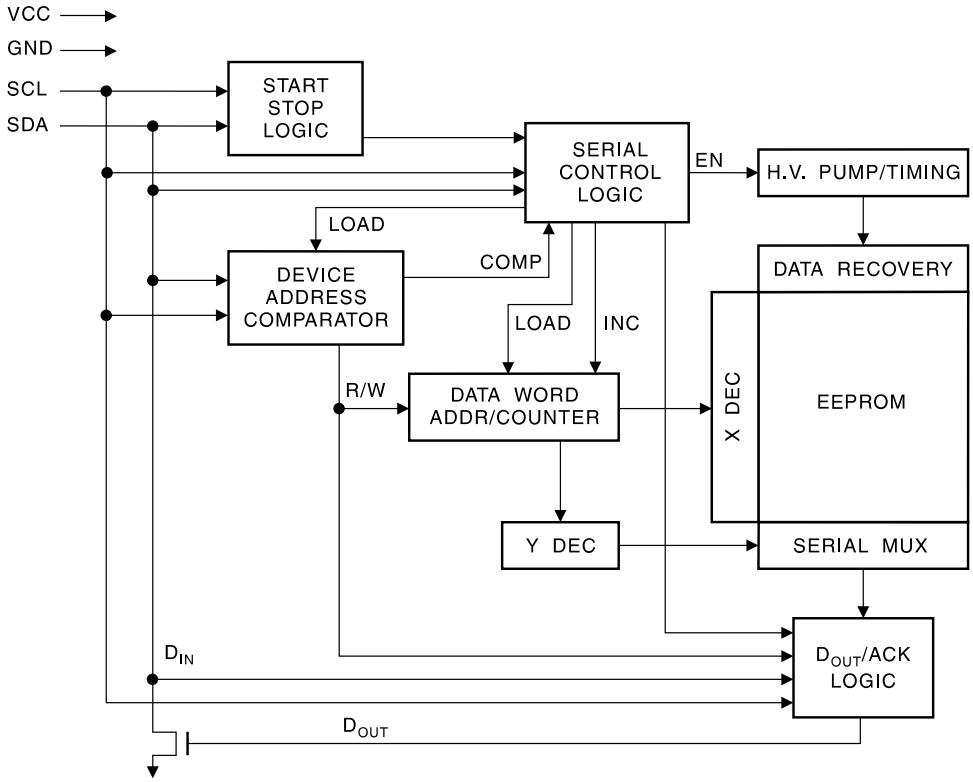
1933B–SEEPR–04/04

Absolute Maximum Ratings*

Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on Any Pin with Respect to Ground	–1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

NOTICE:* Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 2. Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

Memory Organization

AT24C512SC, 512K SERIAL EEPROM: The 512K is internally organized as 512 pages of 128 bytes each. Random word addressing requires a 16-bit data word address.

Pin Capacitance

Table 2. Pin Capacitance[1]
Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +2.7V

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

DC Characteristics

Table 3. DC Characteristics[1]

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC}	Supply Voltage			2.7		5.5	V
I_{CC1}	Supply Current	V_{CC} = 5.0V	Read at 400 kHz		1.0	2.0	mA
I_{CC2}	Supply Current	V_{CC} = 5.0V	Write at 400 kHz		2.0	3.0	mA
I_{SB}	Standby Current	V_{CC} = 2.7V	V_{IN} = V_{CC} or GND			2.0	µA
		V_{CC} = 5.5V				6.0	
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or GND			0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or GND			0.05	3.0	µA
V_{IL}	Input Low Level[2]			–0.6		V_{CC} x 0.3	V
V_{IH}	Input High Level[2]			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Level	V_{CC} = 3.0V	I_{OL} = 2.1 mA			0.4	V

Notes: 1. Applicable over recommended operating range from T_{AC} = 0°C to +70°C, V_{CC} = +2.7V to +5.5V (unless otherwise noted)
2. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Table 4. AC Characteristics[1]

Symbol	Parameter	2.7-volt		5.0-volt		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		400		1000	kHz
t_{LOW}	Clock Pulse Width Low	1.3		0.4		µs
t_{HIGH}	Clock Pulse Width High	1.0		0.4		µs
t_{AA}	Clock Low to Data Out Valid	0.05	0.9	0.05	0.55	µs
t_{BUF}	Time the bus must be free before a new transmission can start[2]	1.3		0.5		µs
$t_{HD.STA}$	Start Hold Time	0.6		0.25		µs
$t_{SU.STA}$	Start Set-up Time	0.6		0.25		µs
$t_{HD.DAT}$	Data In Hold Time	0		0		µs
$t_{SU.DAT}$	Data In Set-up Time	100		100		ns
t_R	Inputs Rise Time[2]		0.3		0.3	µs

Table 4. AC Characteristics[1] (Continued)

Symbol	Parameter	2.7-volt		5.0-volt		Units
		Min	Max	Min	Max	
t_F	Inputs Fall Time[2]		300		100	ns
$t_{SU.STO}$	Stop Set-up Time	0.6		0.25		µs
t_{DH}	Data Out Hold Time	50		50		ns
t_{WR}	Write Cycle Time		5		5	ms
Endurance[2]	5.0V, 25°C, Page Mode	100K		100K		Write Cycles

Note:
1. Applicable over recommended operating range from T_A = 0°C to +70°C, V_{CC} = +2.7V to +5.5V, C_L = 100 pF (unless otherwise noted). Test conditions are listed in Note 3.
2. This parameter is characterized and is not 100% tested.
3. AC measurement conditions:
   R_L (connects to V_{CC}): 1.3 kΩ (2.7V, 5V)
   Input pulse voltages: $0.3V_{CC}$ to $0.7V_{CC}$
   Input rise and fall times: ≤ 50ns
   Input and output timing reference voltages: $0.5V_{CC}$

Device Operation

CLOCK AND DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL-low time periods (see Figure 5 on page 6). Data changes during SCL-high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition that must precede any other command (see Figure 6 on page 7).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (Figure 6 on page 7).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero during the ninth clock cycle to acknowledge that it has received each word.

STANDBY MODE: The AT24C512SC features a low-power standby mode that is enabled upon power-up and after the receipt of the stop bit and the completion of any internal operations.

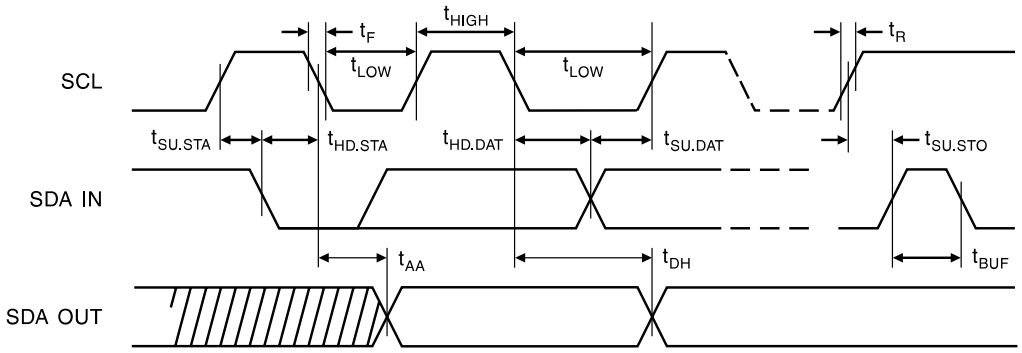
MEMORY RESET: After an interruption in protocol, power loss, or system reset, any two-wire part can be reset by following these steps:

1. Clock up to 9 cycles.
2. Look for SDA high in each cycle while SCL is high.
3. Create a start condition as SDA is high.

Timing Diagrams

Bus Timing

Figure 3. Bus Timing(1)

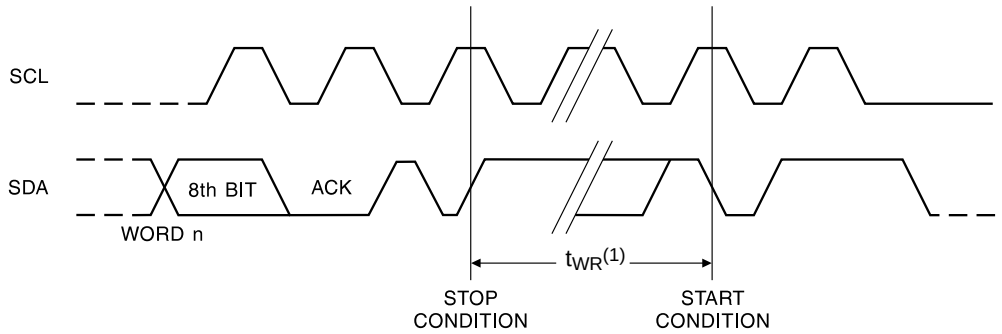


Note: 1. SCL: Serial Clock; SDA: Serial Data I/O

2. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

Write Cycle Timing

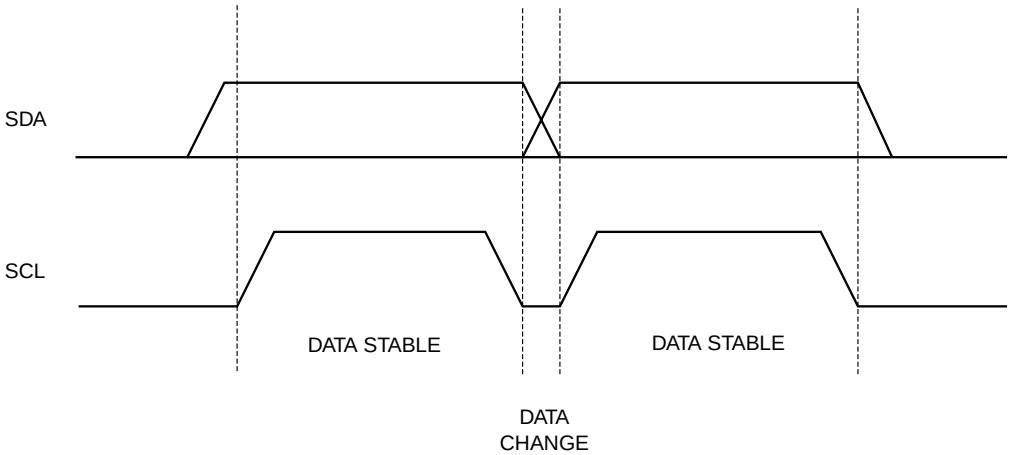
Figure 4. Write Cycle Timing



Note: 1. SCL: Serial Clock; SDA: Serial Data I/O

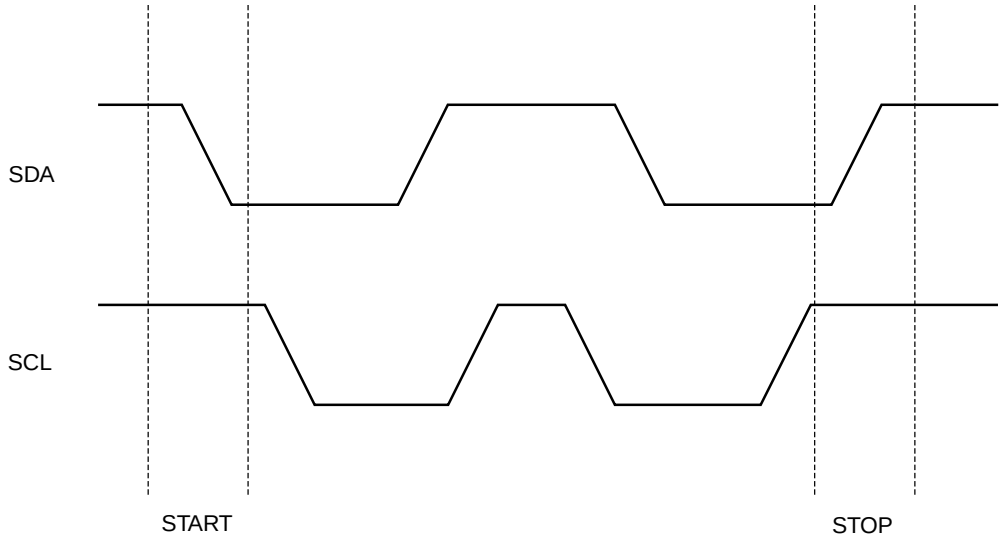
Data Validity

Figure 5. Data Validity



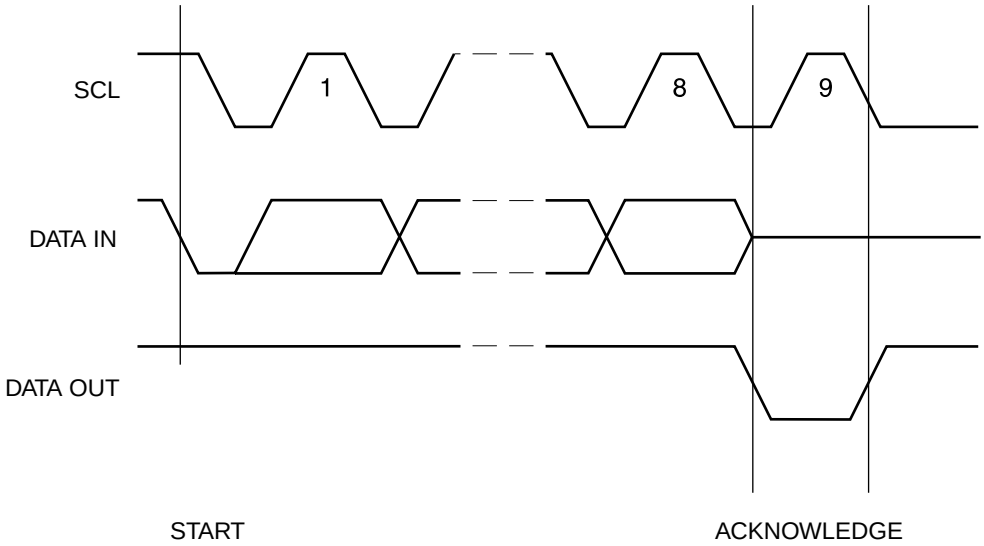
Start and Stop Definition

Figure 6. Start and Stop Definition



Output Acknowledge

Figure 7. Output Acknowledge



Device Addressing

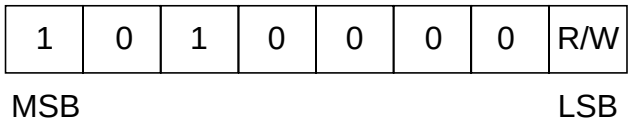
The 512K EEPROM requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (see Figure 8). The device address word consists of a mandatory “one, zero” sequence for the first four most significant bits as shown. This is common to all two-wire EEPROM devices.

The next three bits of the device address word are unused. These three unused bits should be set to “0”.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a “0”. If a compare is not made, the device will return to a standby state.

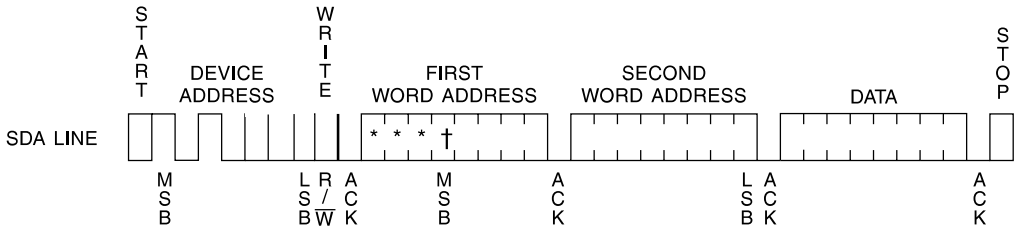
Figure 8. Device Address



Write Operations

BYTE WRITE: A write operation requires two 8-bit data word addresses following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a “0” and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a “0”. The addressing device, such as a microcontroller, then must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see Figure 9).

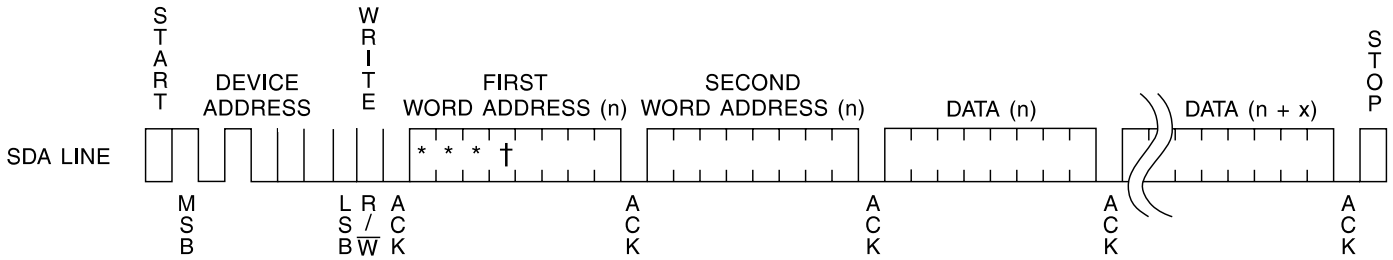
Figure 9. Byte Write



PAGE WRITE: The 512K EEPROM is capable of 128-byte page writes.

A page write is initiated the same way as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 127 more data words. The EEPROM will respond with a “0” after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see Figure 10).

Figure 10. Page Write



The lower seven data word address bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 128 data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten. The address “roll over” during write is from the last byte of the current page to the first byte of the same page.

ACKNOWLEDGE POLLING: Once the internally-timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a “0”, allowing the read or write sequence to continue.

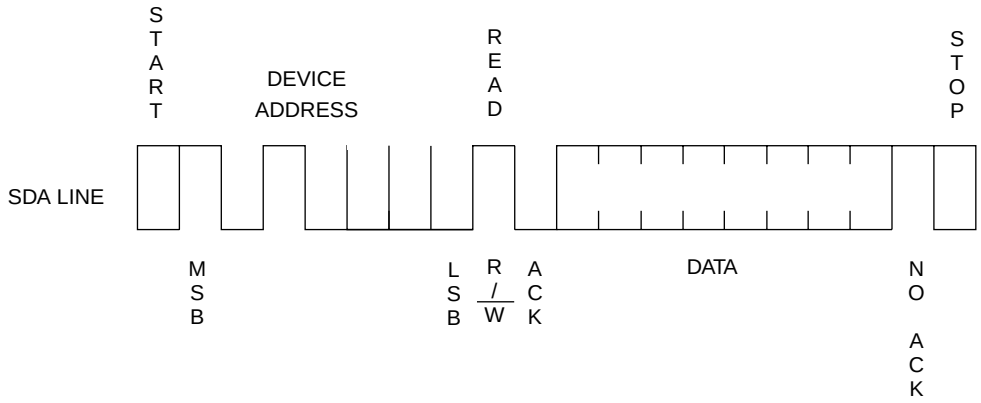
Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address “roll over” during read is from the last byte of the last memory page to the first byte of the first page.

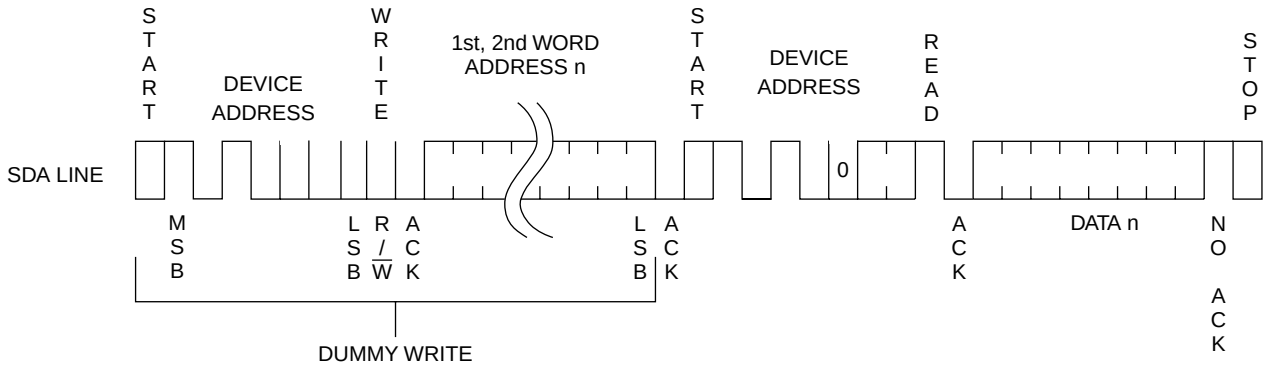
Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input “0” but does generate a following stop condition (see Figure 11).

Figure 11. Current Address Read



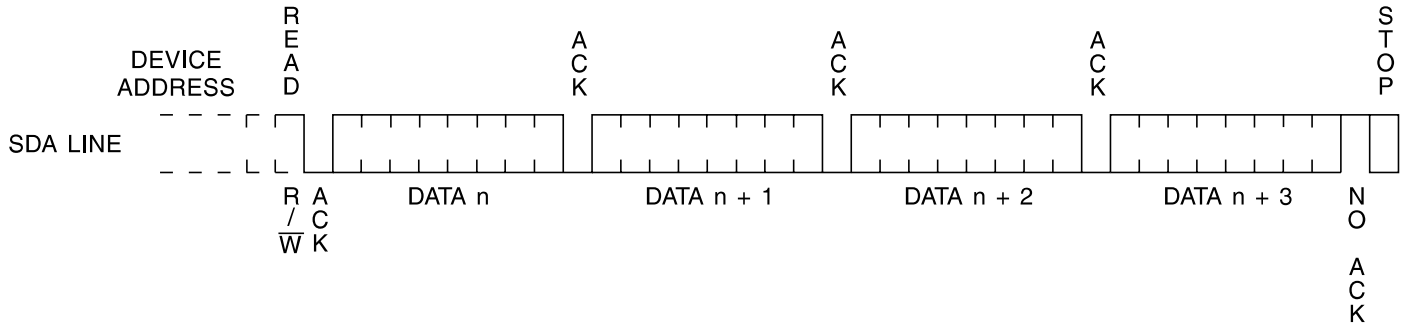
RANDOM READ: A random read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a “0” but does generate a following stop condition (see Figure 12).

Figure 12. Random Read



SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will “roll over” and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a “0” but does generate a following stop condition (see Figure 13)

Figure 13. Sequential Read.



AT24C32SC Ordering Information

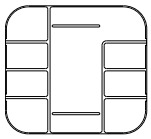
Ordering Code	Package[1]	Voltage Range	Temperature Range
AT24C512SC-09LT	M2 – L Module	2.7V–5.5V	Commercial (0°C–70°C)
AT24C512SC-09AT	M2 – L Module	2.7V–5.5V	Commercial (–40°C–70°C)

Package Type[1]	Description
M2 – L Module[2]	M2 ISO 7816 Smart Card Module

Note: 1. Formal drawings may be obtained from an Atmel sales office.
2. Atmel currently offers this device in the “L” module only.

Smart Card Module

Ordering Code: 09LT



Module Size: M2
Dimension(1): 12.6 x 11.4 [mm]
Glob Top: Square: 8.6 x 8.6 [mm]
Thickness: 0.58 [mm] max
Pitch: 14.25 [mm]

Note: The module dimensions listed refer to the dimensions of the exposed metal contact area. The actual dimensions of the module after excise or punching from the carrier tape are generally 0.4 mm greater in both directions (i.e., a punched M2 module will yield 13.0 x 11.8 mm).

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